Written Exam | IH1611 Semiconductor Devices | Friday, March 18, 2022

Duration 5 hours, 8-13

Handwritten solutions

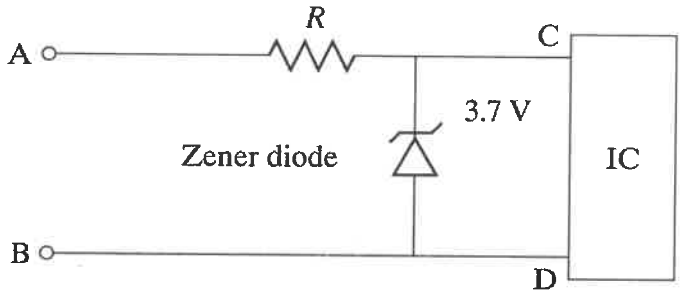
Write clearly and draw figures according to the instructions!
Sign your name on all answer sheets!
Use a new sheet for every task.
Examiner and responsible teacher: Gunnar Malm, 08-790 43 32

The student may use the following items during the exam: Calculator, ruler, and the attached "Material Properties and Formulas, version spring 2020"

Structure: *The exam consists of six tasks. To pass the exam you should fulfill the grading criteria to E level. Each task assesses one or two criteria. Carefully read and consider all tasks at the start of the exam.*

Students who do not pass the exam, but according to the judgment of the examiner have met most criteria, will be offered one opportunity to complement their exam on task level so that the overall criteria are fulfilled.

Task 1 Applications of semiconductor devices and CMOS integrated circuits



Assume that the integrated circuit (IC) in the figure above is fabricated using a relatively old generation of CMOS-technology with 3 nm gate oxide thickness.
Is the choice of a 3.7 V zener diode appropriate to protect the circuit from electrostatic discharge (ESD) i.e. high voltage pulses/transients appearing between the terminals A & B? Given: the critical field for silicon dioxide (SiO_2) breakdown is $\mathscr{E}_{crit} = 10$ MV/cm?

Solution:

Find the field by calculating

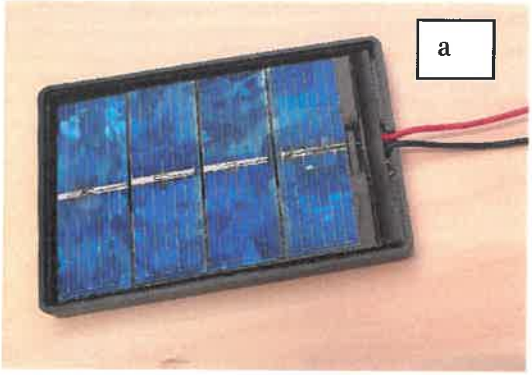
$$\mathcal{E} = \frac{V_{zener}}{t_{ox}} = \frac{3{,}7V}{\underbrace{3 \cdot 10^{-7}\,cm}_{=3nm}} = 12{,}3\,MV/cm$$

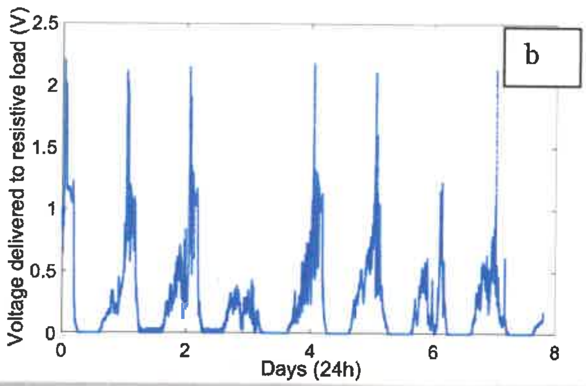
$> \mathcal{E}_{crit}$

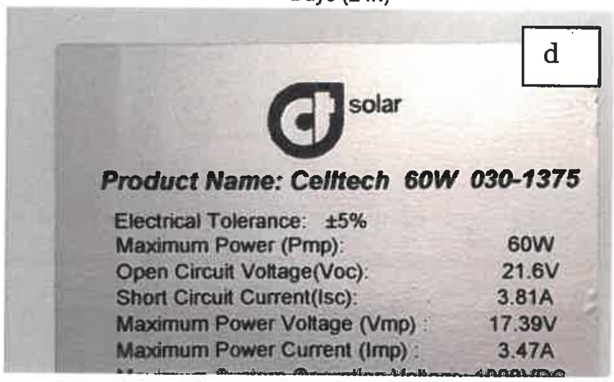
The conclusion is that the diode cannot fully protect the oxide. Any pulse with amplitude above 3V would be too high

The task is approx. at C-level. Involves some semiconductor concepts, such as tox but mainly basic electrostatics. The working principle of a Zener-diode is useful but not essential to solve this task.

Task 2 Solar Cells







The pictures a)-d) show two different semiconductor based solar cells/panels. The small solar cell a) was characterized by connecting it to a suitable resistive load and a data logger.

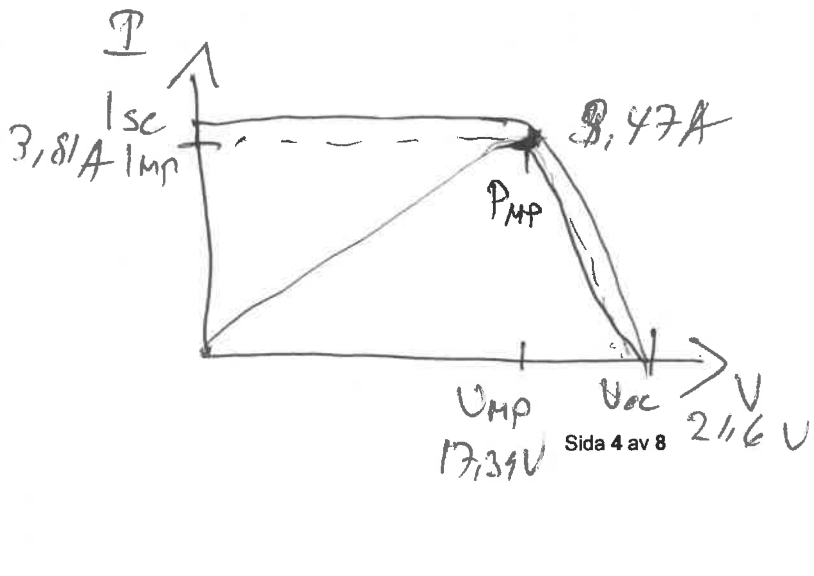
- Based on the photo a) and the recorded data b) explain which semiconductor material that was used and how the solar cell equivalent circuit connection affects the output voltage. What else can you tell from the recorded data over time?
- The photo of a large solar cell c) shows several wafers mounted to form a ~ 1×1 m^2 panel. Explain the different values that are given in the photo of the panel label d). Draw a suitable graph and indicate the values in the correct locations. What is the most likely wafer material?

Solution

The photo a) shows a material with varying colors and some shapes within the layer. Hence, the material is either amorphous or polycrystalline. The panel b) indicates that a few cells are connected in series since an E_g of Si 1,12 eV gives open-circuit voltage around half the bandgap (0,7 V). In summary amorphous silicon seems like a possible candidate

The second question c) shows silicon wafer mounted in a 4 x 4,5 array.

The basic solar cell IV is plotted like below



C-A level depending on completeness of answer

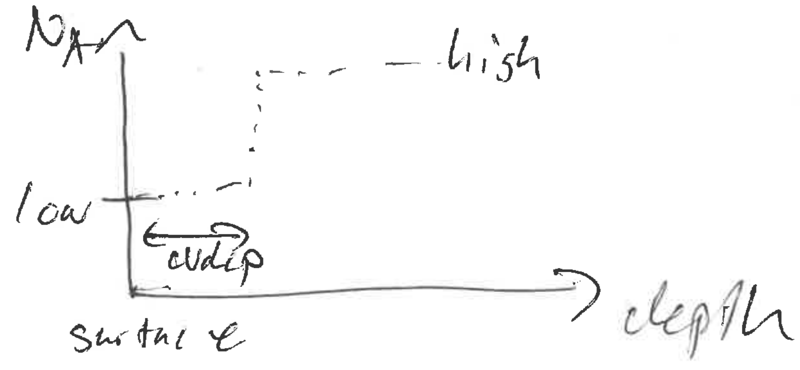
Task 3 Device physics (MOSFET)

Explain at least one benefit or consideration that motivates the use of a retrograde channel doping profile in a MOSFET transistor? Hint: a lower doping is used at the surface and a higher doping is used in the bulk/body.

The basic MOSFET IU relation reads

$$I_{ds} = \frac{W}{L} \mu_{ns} C_{ox} \left(U_{GS} - U_T - \frac{m U_{ds}}{2} \right) U_{ds} \quad (*)$$

In (*) the surface mobility μ_{ns} benefits from a low doping, the U_T can be set to a value that is not too high and the body factor m is controlled by the higher doping mainly, since Wdep becomes "fixed"



A-level task since detailed knowledge of physics and fabrication schemes are used

Task 4 Device physics (band diagrams)

Use band diagram drawings to explain why pn-junction diodes and Schottky diodes are suitable for different applications.

- Your band diagrams should be drawn with correct scales for the locations of the Fermi levels. Assume typical values for material parameters e.g. from the lab exercise if applicable. Both types of diodes are fabricated on silicon wafers.
- Name at least one typical application for each diode type.

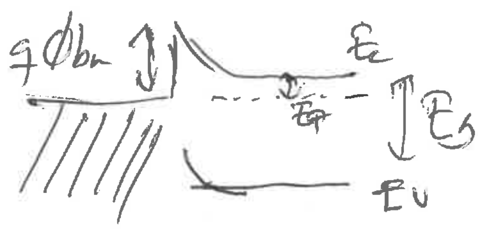
First note that Schottky diodes are lowly-doped

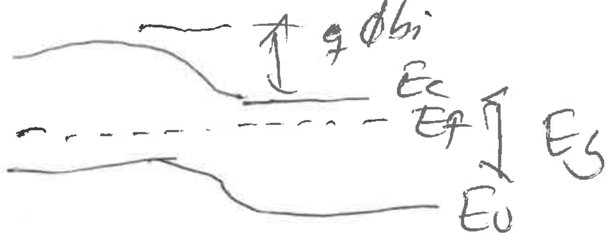
assume $N_{A,D} \sim 10^{17} cm^{-3}$ or lower

PN-junction are assymetrical with N_A/N_D ratio of at least x1000 e.g. $N_{A,D} = 10^{20} cm^{-3}$, $N_{D,A} = 10^{17} cm^{-3}$, Assume equilibrium ⇒ Fermi level is constant / flat

Schottky on n-type

PN





C-level

PN-diode is used in LEDs, and image detectors, , ... —

Schotty mainly in AC/DC rectifiers high I, low U

Also C-level

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Task 5 CMOS inverter

What happens to the gate delay if the threshold voltage (V_T) is raised by 100 mV (absolute value) for both NMOS and PMOS transistors in a CMOS inverter? Make reasonable assumptions for modern CMOS technology nodes for e.g. voltage levels. Your answer can be given as a relative change (%).

Gate delay eq:

$$\tau d \approx \frac{CVdd}{4}\left(\frac{1}{I_{ON}} + \frac{1}{I_{ONP}}\right)$$ if NMOS and

PMOS drive strength is balanced by $W_P \approx 4 \times W_N$

then

$$\tau d \approx \frac{CVdd}{2}\left(\frac{1}{I_{ON}}\right)$$

Above U_T then $I_{ds} \propto (U_{gs} - U_t)$ gate overdrive

in linear region, while in saturation

$I_{ds} \propto (U_{gs} - U_t)^2$. Use saturation and

assume $U_{gs} \approx 1{,}0$ and $U_{T\,low} = 0{,}3\,U$

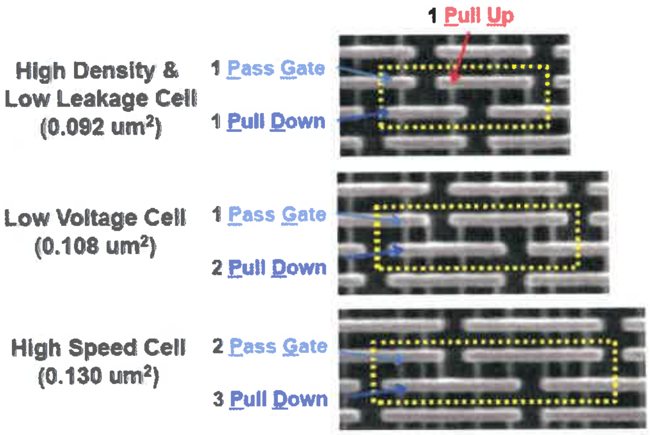
$U_{T\,high} = 0{,}3 + 0{,}1 = 0{,}4\,U$

Since $\tau d \propto \frac{1}{I_{ON}}$ then ratio becomes

$$\frac{\tau d_{high}}{\tau d_{low}} \sim \frac{(1{,}0 - 0{,}3)^2}{(1{,}0 - 0{,}4)^2} = 1{,}36 \Rightarrow 36\%$$ increase

A-level since multiple ~~steps~~ steps at device & circuit level

Task 6 Semiconductor memories and modern technology nodes



The picture shows three different memory cell layouts in Intel 22 nm FinFET technology.

a) What is the memory cell type called and where is it used?
b) How does this cell achieve a stable memory state?
c) What is meant by pull-up and pull-down respectively and why are their ratios different in the three given cells? Your answer should compare transistor sizing in planar CMOS and FinFET technology respectively you do not have to explain the memory cell operation in detail for this sub task.

The 6T configuration with pull-up and pull-down paths in cross-coupled inverters and pass-gates is known as static RAM i.e. SRAM for short. Stability in ensured by connecting inverter outputs to inputs. Very strong pass-transistors are needed to alter this state

Pull up are the inverter PMOS devices connected to supply voltage VDD and pulldown is NMOS conn. to GND. In SRAM you want minimum density which is single FIN3 or minimum widths in planar technology respectively.

A-level since "modern technology"