Duration 5 hours, 8-13

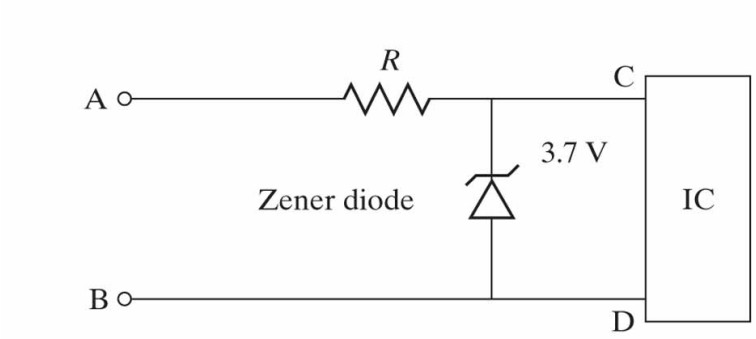
Write clearly and draw figures according to the instructions!
Sign your name on all answer sheets!
Use a new sheet for every task.
Examiner and responsible teacher: Gunnar Malm, 08-790 43 32

The student may use the following items during the exam: Calculator, ruler, and the attached ”Material Properties and Formulas, version spring 2020”

Structure: *The exam consists of six tasks. To pass the exam you should fulfill the grading criteria to E level. Each task assesses one or two criteria. Carefully read and consider all tasks at the start of the exam.*

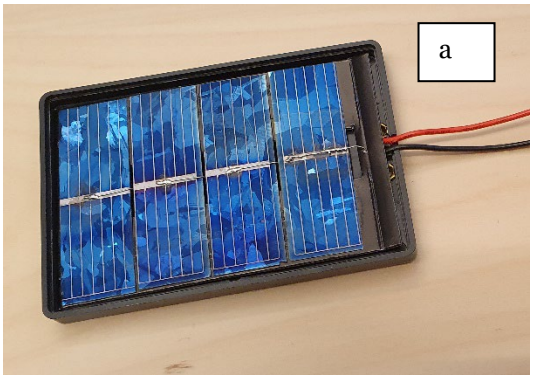
Students who do not pass the exam, but according to the judgment of the examiner have met most criteria, will be offered one opportunity to complement their exam on task level so that the overall criteria are fulfilled.

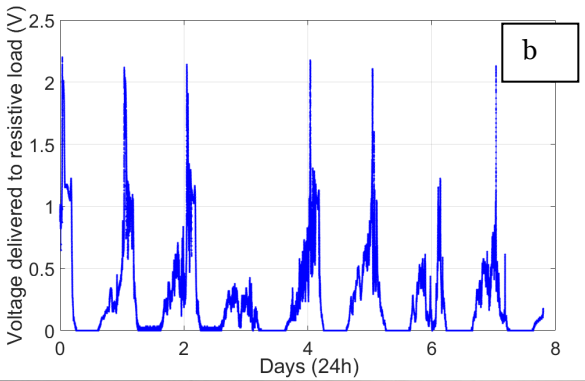
Task 1 Applications of semiconductor devices and CMOS integrated circuits

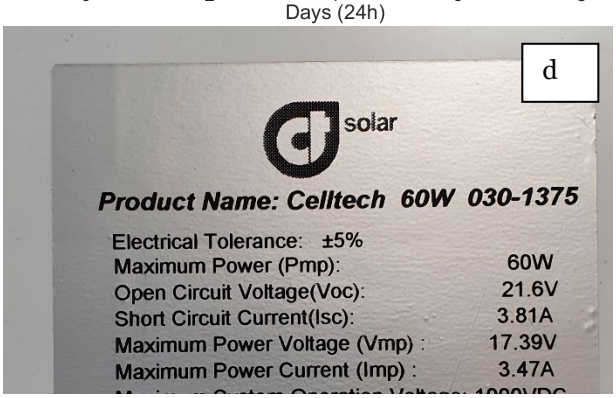


Assume that the integrated circuit (IC) in the figure above is fabricated using a relatively old generation of CMOS-technology with 3 nm gate oxide thickness.
Is the choice of a 3.7 V zener diode appropriate to protect the circuit from electrostatic discharge (ESD) i.e. high voltage pulses/transients appearing between the terminals A & B?
Given: the critical field for silicon dioxide (SiO_2) breakdown is $\mathscr{E}_{crit}$ = 10 MV/cm?

Task 2 Solar Cells







The pictures a)-d) show two different semiconductor based solar cells/panels. The small solar cell a) was characterized by connecting it to a suitable resistive load and a data logger.

- Based on the photo a) and the recorded data b) explain which semiconductor material that was used and how the solar cell equivalent circuit connection affects the output voltage. What else can you tell from the recorded data over time?
- The photo of a large solar cell c) shows several wafers mounted to form a ~ 1 × 1 m^2 panel. Explain the different values that are given in the photo of the panel label d). Draw a suitable graph and indicate the values in the correct locations. What is the most likely wafer material?

Task 3 Device physics (MOSFET)

Explain at least one benefit or consideration that motivates the use of a retrograde channel doping profile in a MOSFET transistor? Hint: a lower doping is used at the surface and a higher doping is used in the bulk/body.

Task 4 Device physics (band diagrams)

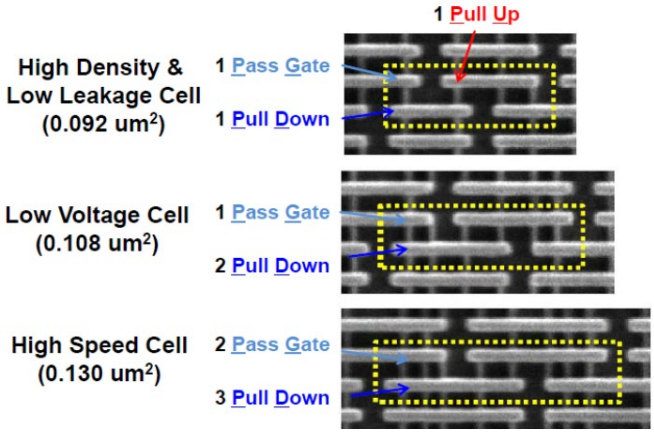
Use band diagram drawings to explain why pn-junction diodes and Schottky diodes are suitable for different applications.

- Your band diagrams should be drawn with correct scales for the locations of the Fermi levels. Assume typical values for material parameters e.g. from the lab exercise if applicable. Both types of diodes are fabricated on silicon wafers.
- Name at least one typical application for each diode type.

Task 5 CMOS inverter

What happens to the gate delay if the threshold voltage (V_T) is raised by 100 mV (absolute value) for both NMOS and PMOS transistors in a CMOS inverter? Make reasonable assumptions for modern CMOS technology nodes for e.g. voltage levels. Your answer can be given as a relative change (%).

Task 6 Semiconductor memories and modern technology nodes



The picture shows three different memory cell layouts in Intel 22 nm FinFET technology.

a) What is the memory cell type called and where is it used?
b) How does this cell achieve a stable memory state?
c) What is meant by pull-up and pull-down respectively and why are their ratios different in the three given cells? Your answer should compare transistor sizing in planar CMOS and FinFET technology respectively you do not have to explain the memory cell operation in detail for this sub task.